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[54]	INSULATED GATE FIELD EFFECT
	TRANSISTOR HAVING GUARD RING
	REGIONS

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[30]

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	H01L 23/58		
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	257/173; 257/368; 257/487; 257/488; 257/490		
[58]	Field of Search 257/139, 147,		
- -	257/153, 170, 173, 487–490, 355, 368		

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[57] **ABSTRACT**

An insulated gate field effect transistor comprising a semiconductor substrate having one side on which a cell area is composed of a plurality of first wells of a first conductivity type, each of the first wells containing a source region of a second conductivity type. A channel region is defined in the surface portion of the semiconductor substrate adjoining to the source region, and a gate electrode is formed, via a gate insulating film, at least over the channel region. A source electrode is in common contact with the respective source regions of the plurality of first wells. The semiconductor substrate has a drain electrode provided on another side. A current flows between the source electrode and the drain electrode through the channel being controlled by a voltage applied to the gate electrode. A guard ring area is disposed on the one side of the semiconductor substrate so as to surround the cell area. The source electrode has an extension connected to a second well of a second conductivity type formed in the one side between the cell area and the guard ring area to provide a by-pass such that, when a current concentration occurs within the guard ring area, the concentrated current is conducted directly to the source electrode in the cell area through the by-pass, thereby preventing the concentrated current from causing a forward biassing between the first wells and the source region.

19 Claims, 17 Drawing Sheets

